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Novel electric arc current emulation system for low-voltage grids

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ABSTRACT

An electric arc is a common distribution grid error, even more so with the use of electric vehicles and renewable energy sources that increase the likelihood of grid errors. Several control systems and strategies are under development to minimize electric-arc faults and to guarantee reliable grid performance. All the control strategies must be validated through emulations of the different fault modes at laboratory scale where there is no risk to either the researchers or the facilities. In this study, a novel system is proposed for the emulation of electric arc current waveforms, based on both real measurements and equation-based modeling. The proposed modular system provides the capability to emulate different levels of arcing currents. Validation of the system was demonstrated, in view of the design, the underlying theoretical analysis, and a set of control system simulations and experiments.

1. Introduction

Several factors such as the increasingly widespread use of electric vehicles and self-consumption systems, as well as the connection of storage systems can disrupt reliable performance of the electric distribution grid. These new factors can interrupt grid stability, provoking electrical faults that drastically diminish electricity supply quality. In most cases, those electrical faults generate arcs between one of the phases and the ground [1]. Several factors, such as time and arc distance define the electric arc and its characteristics [1,2]. Accurate modeling of electric arcs is crucial, as their effects on the grid can be studied, before implementing fault detection algorithms [3], and testing appropriate protective devices [4], among other points.

Real electric arcs pose a risk to people and equipment due to the high currents and high temperatures that are generated when an arc occurs, even in Low Voltage (LV) devices. All these problems can be avoided when software tools are used that simulate the behavior of electric arcs in safe and suitable ways. To do so, several models representing the different properties of electric arcs and their performance have been developed [5–8].

In some cases, software tools have been used to validate the models developed for the characterization of electric arcs [9], particularly algorithms for testing fault-detection systems [10,11]. Furthermore, experimental validation is sometimes conducted at LV facilities, using a resistance value [12–14] in substitution of a real electric arc. However, the non-linearity of a real electric arc is not accurately replicated.

Medium Voltage (MV) facilities with real electric arcs have been used for experimental validation of arc events [3,15,16]. Some authors emulate a High Impedance Arc Fault (HIAF) that is a common fault type in MV distributions grids by using a tree branch [17,18]. However, these require expensive equipment, special safety rules, and even large outdoor premises. Facilities to which many research centers and universities will not have access. In [19,20], the arc is also substituted by a fixed resistance that neglects the non-linearity of the electric arc.

The generation of an electric arc on an LV test bench has also been reported [21] for selecting the parameters of the black-box model. In [22–25], an LV arc generator was used to collect data for arc-detection algorithms. However, the parameters of the arc profiles that were generated were often poorly adjusted, as only the distance between the electrodes can be modified. In [26], real arcs were generated with a tree branch as a fault resistance, producing arcs that varied between experiments. Additionally, the random occurrences of each arc form could not be predicted. In [25,27], an arc is generated by placing two cables alongside each other with a small insulator gap to simulate an insulation fault. It is a standard test in IEC 62606 [28] for the arc fault detection devices installed in residential LV grids.

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Nomenclature

τ	Time constant of the electric arc
DUR	Dist-C model parameter for regulating duration
EXT	Dist-C model parameter for regulating extension
$FPGA$	Field Programmable Gate Array
g	Electrical conductance (1/R)
$HIAF$	High Impedance Arc Fault
I_{arc}	Arc current instant value
IAE	Integral of the Absolute magnitude of the Error
LV	Low Voltage
$MOSFET$	Metal-Oxide-Semiconductor Field-Effect Transistor
MV	Medium Voltage
OFS	Dist-C model parameter for regulating offset
P_0	Arc loss constant
PCB	Printed Circuit Board
PWM	Pulse-Width Modulation
RC	Resistor–Capacitor
T_{case}	MOSFET case temperature
T_{junct}	MOSFET junction temperature
U_{arc}	Voltage instant value in the arc
U_c	Constant arc voltage

This study proposes a new LV Printed Circuit Board (PCB) to emulate the arc current waveform. The proposed system can be implemented in any LV installation, thereby facilitating research into grid faults and the development of system prototypes with more realistic behaviors. Its main contributions are:

- Emulation of electric arcs at LV facilities without endangering people or facilities. In some studies, there is a real fire hazard when a real arc is generated, that should be noted.
- Configurable parameters: a wide variety of current waveforms can be generated.
- Compact and low-cost solutions.
- Modular solutions: the proposed system is parallelizable, increasing current levels, as may be desired.

The rest of this paper is organized as follows: In Section 2, the theoretical models for electric arcs are defined. Then, in Section 3, the proposed PCB array is described. The performance of the PCB array is simulated in Section 4. The experimental results are then presented in Section 5. In Section 6, the proposed system is compared with other systems in LV and, finally, the conclusions are summarized in Section 7.

2. Theoretical models for electric arcs

Most electric-arc models can be classified into the following two categories [29]. Physical models: the most complex type, based on the conservation of mass, momentum, and energy. Black-box models: a straightforward way of comprehending the fundamental characteristics of an electric arc and its interactions with the surrounding environment.

While black-box representations are a simplification that cannot capture the full complexity of an arc, they are useful in the design and analysis of arc-based systems [30] and are widely used. Among them, both Cassie and Mayr each proposed an arc model based on commonly employed differential equations [5,31]. There are, in addition, a number of black-box models such as those of Habedank, Schwartz, and Schavemaker that are also based on either the Cassie or the Mayr model [30]. Some variations were also proposed when both models were arranged in series or parallel arrays and some of the parameters were considered non-constant [6–8]. Most black-box models have two dependent parameters, such as τ and U_c in the Cassie and τ and P_0 in the Mayr model [5–8,31]. In [15], a High Impedance Arc Fault (HIAF) with three tuneable parameters, based on the heat balance equation, was also proposed. In some studies, *i.e.*, [32], electric arc furnaces are modeled using artificial neural networks. However those models are difficult to reproduce.

Both the Cassie and the Mayr models, as well as the Dist-C [15] model are described below.

2.1. The Cassie and the Mayr arc models

Both the Cassie and the Mayr models are based on a differential equation of arc conductivity [5,31]. However, some simplifications are assumed in each model. In Cassie's model, it is assumed that the arc temperature, current density, and electric field are all constants, and the main energy removal mechanism is convection. In the Mayr model, a uniform arc cross-section and constant cooling power are assumed. The main energy removal mechanism in this model is radial-thermal conduction.

The differential equations in both cases are as follows:

$$\frac{1}{g}\frac{dg}{dt} = \frac{(f(model)-1)}{\tau}, \tag{1}$$

where $f(model) = U_{arc}^2/U_c^2$ for Cassie and $f(model) = U_{arc}I_{arc}/P_0$ for Mayr.

2.2. The Dist-C model

Another noteworthy option is the Dist-C model which is an HIAF model [15]. The non-linear component of the arc is described by modeling it with two resistors, one linear, the other non-linear, connected in series.

Based on the heat balance equation, the non-linear resistance is calculated as:

$$R_{nln} = e^{\int \frac{1}{\tau}P_{res}(t)\,dt}, \tag{2}$$

where $P_{res}(t)$ is:

$$P_{res}(t) = K_1\left(t - T_d - \frac{DUR}{2}\right) - b_1,$$
$$t \in \left[T_d - \frac{DUR}{2}, T_d + \frac{DUR}{2}\right], \tag{3}$$

and where:

$$K_1 = -\frac{8ln(EXT)}{DUR^2},$$
$$b_1 = \frac{4ln(EXT)}{DUR}, \tag{4}$$

in which T_d is the time within which R_{nln} reaches its maximum value. It can be modified by changing the offset regulation parameter OFS. Once obtained, the value of R_{nln} is added to the linear resistor R_{ln}. The arc voltage is divided by the total resistance to obtain the arc current. So, the three parameters DUR, OFS, and EXT have an important impact on the duration, offset, and magnitude of the current distortions. One advantage of the Dist-C model is the independence of its three parameters from one another, making them easy to tune. More detailed information on the Dist-C model is available in [15].

It has to be borne in mind that a stochastic component is always present in a real arc. However, that stochastic behavior is not always foreseen in all arc models. An existing arc model can nevertheless be modified, in order to consider that stochastic behavior [3]. In addition, if the valve effect has to be considered [33], different gains can be applied to the positive and negative semi-cycles of the current. Finally, another option for recreating real arcs is to take data collected from the distribution network. It is an interesting option, as the real electric arc waveforms can be taken into account, as will be shown later on.

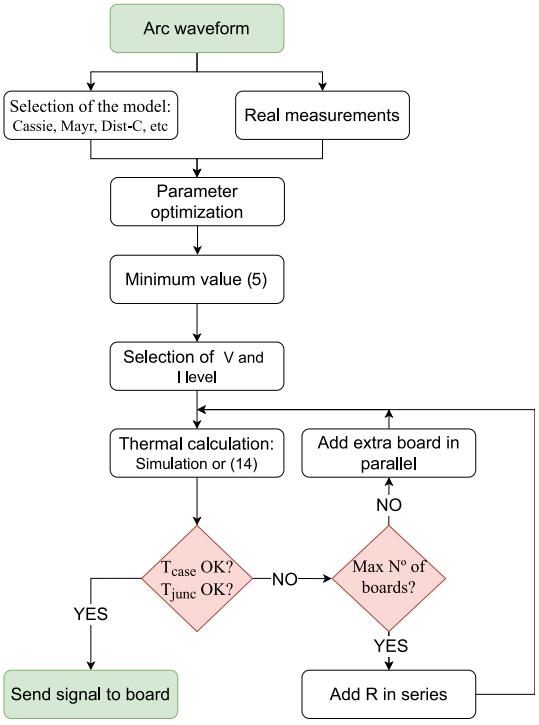


Fig. 1. Flow chart proposed for obtaining the number of PCBs and arc waveforms.

3. Novel system for emulating electrical arc currents

Arcs can be safely emulated with the proposed system with which a diverse range of voltages and currents can be used. The process to obtain both the arc waveforms and the PCB components, thermal model, *etc*. are explained in this Section and summarized in Fig. 1.

3.1. Extraction of the arc model based on real data

As discussed in Section 2, there are two main approaches to emulate arc current waveforms. Those parameters can be modeled with suitable equations using one of the existing theoretical arc models (Cassie, Mayr, *etc*.) or considering real measurements of electric faults.

Either of the two above options can be considered in the proposed solution. In this study, actual data were updated to develop a practical solution, based on measurements of electric faults in the MV distribution lines of i-DE (Iberdrola Group) [34], a grid distribution system operator in Spain. It is worth noting that only single-phase to ground faults were considered, which represent almost 80% of all faults [35]. Furthermore, the actual electric fault is normalized, as the distribution power lines under study have different voltage levels ranging from 13 kV to 30 kV. Once normalized, the data are used as a baseline to obtain the parameters of the arc models presented in Section 2. The two main arc models, the Cassie and the Mayr models [30,36], together with the HIAF model in [15] were selected for this study, in order to develop some examples of the proposed system. The arc-model parameter values were obtained through comparisons between real arc data and the current waveforms of theoretical models. Iterative processing of a genetic algorithm [37] facilitated this comparison.

The best parametric combination was evaluated using the Integral of the Absolute magnitude of the Error (IAE) or the Integral Square Error (ISE) within a single period:

$$IAE = \int_0^T |\, e(t) \,|\, dt \qquad or \qquad ISE = \int_0^T e(t)^2 dt, \tag{5}$$

where $e(t) = i_{real}(t) - i_{model}(t)$.

Thus, the objective was to obtain the best parameters of the arc model that minimized the value of the IAE or ISA, so that the model-generated waveform resembled the waveform of the real measured faults. The results obtained with both indicators were equivalent.

The behavior of an arc depends on several factors, including the arc voltage and the dielectric withstand voltage [38]. These factors impart a singularity to each arc that can be described as non-linear, asymmetric, and random [39]. It is therefore important to note, in order to emulate the behavior of any electric arc in LV facilities that, if both the voltage and the current have the same polarity, then the proposed solution and configuration can be used to reproduce any current waveform.

Once the parameters of the arc models are obtained, it is desirable to use them on test platforms, in order to emulate electric arcs and to use them for multiple purposes such as the design of new control systems, and testing new equipment during grid faults, *etc*. The following subsection describes the development of the PCB for the emulation of electric arc models.

3.2. Design of the PCB

Electric faults that interrupt grid distribution lines involve such high levels of voltage and current that testing is unfeasible at most research facilities. Additionally, generating real electric arcs poses a risk to both personnel and facilities. Thus, to validate protection schemes and to test controls during electric faults, it is more feasible to emulate electric arcs on scaled-down prototypes where the power levels used are lower than those found in a mains distribution grid.

In this paper, the design of a PCB was proposed, based on a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) working in the ohmic region. In this operating mode, the MOSFET acts as a variable resistor, which is key to emulate the non-linearities of an arc current. It enables the secure emulation of any resistive current waveform type, regardless of the arc model employed in the prototype. In addition to the models described in Section 2, other existing arc model could be used. The proposed PCB electrical diagram, in which the main signals are highlighted, is presented in Fig. 2, to enhance comprehension of its functionality.

Each PCB was based on a single MOSFET working in the linear region. As there was a single MOSFET, the current reference (Fig. 2, ①I^{ref}) was the absolute value of the current generated with the arc model, which was introduced into the 5th pin of the operational amplifier. The resistor voltage drop (Fig. 2, R_{shunt}) was then introduced in the 6th pin as a feedback, creating a closed-loop. The resulting signal was proportional to the current that was passing through R_{shunt}. The operational amplifier will change the setpoint of the MOSFET, if the error is not equal to zero, until the desired value is reached. In that way, the current flowing through the resistor, R_{shunt}, will be equal to the arc current reference (Fig. 2, ①I^{ref}) sent to the PCB.

As the current through the MOSFET was always positive while the arc current was alternating, a full-bridge rectifier was employed to rectify the input voltage (Fig. 2, ③V_{input}) of the PCB. In doing so, the voltage in the MOSFET (Fig. 2, ④V_{rec}) remained consistently positive, maintaining the current at all times with the same polarity through the MOSFET. However, the current in the grid (Fig. 2, ②I_{arc}) was AC and had the same polarity as the grid voltage.

The PCB was designed to work with a maximum peak current of $I_{peak} = 2$ A and a voltage level of $V_{input}^{peak} = 125$ V. If higher currents are needed, multiple PCBs can be arranged in parallel. Conversely, if higher voltage levels are required, the current level *per* PCB can be reduced or resistance can be added at the input, to limit the maximum power dissipated by the MOSFET. Those limits are analyzed in the following subsection.

3.3. Thermal limits of the system in steady-state

It is important to analyze the thermal limits of the PCB to ensure good system performance. In this case, the main limitation is the

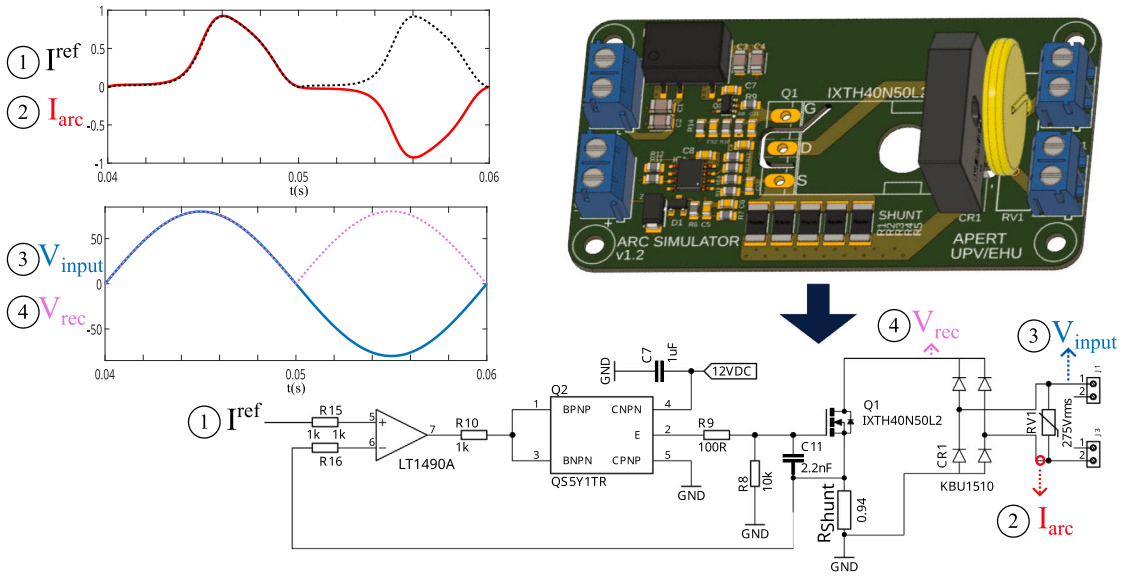


Fig. 2. Representation and electric diagram of the proposed PCB with the main signals.

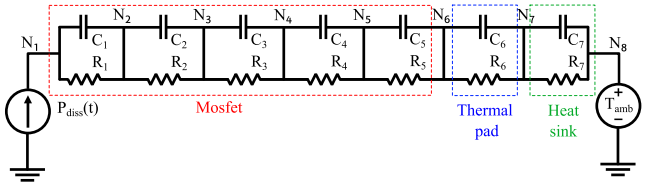


Fig. 3. Foster thermal model of the PCB design.

Table 1
Thermal conduction and electrical transmission variable analogy.

Thermal		Electrical	
Temperature	T [K]	Voltage	V [V]
Heat flow	P [W]	Current	I [A]
Thermal resistance	R_{th} [K/W]	Resistance	R [Ω]
Thermal capacitance	C_{th} [Ws/K]	Capacitance	C [As/V]

amount of power that each MOSFET can dissipate. Excessive power dissipation will increase T_{junct} and T_{case}, which will cause the PCB to malfunction. It is imperative that T_{junct} should remain below the manufacturer's maximum recommended limit, in order to ensure proper operation of the MOSFET. However, direct measurement of T_{junct} was unfeasible, due to its physical unavailability. Therefore, in this paper, the average value of T_{case} in steady-state was the only temperature that could be feasibly measured. It was used to validate the Foster model Fig. 3, by comparing both the experimental and the modeled average T_{case} values, in order to ensure the accuracy of the T_{junct} value obtained with the model. Those limits were used to calculate whether the PCB was capable of withstanding the required current and voltage. If $T_{case_{calc}} > T_{case_{max}}$ and $T_{junct_{calc}} > T_{junct_{max}}$, additional PCBs must be added in parallel Fig. 1, to reduce the current per PCB and therefore the power dissipation in the MOSFET.

Tests and complex finite-element simulations can be set up, to assess the T_{case} of semiconductors [40]. However, it is preferable to use simple and compact simulation-based models that save time [41]. A considerable number of those compact thermal models were expressed as thermal Resistor–Capacitor (RC) networks. If the RC model parameters are accurately calculated, the precision achieved with those networks is satisfactory, and computational times are significantly shorter than more demanding methods [41,42]. There are two main types of RC networks: Foster networks and Cauer networks. Foster networks are invariably found in component data sheets, therefore in this paper a Foster network Fig. 3 is used to estimate T_{junct} and T_{case} average values once the steady state is achieved in the MOSFET.

Using the analogy between thermal conduction and electrical transmission Table 1, the worst case average, T_{case}, neglecting the effect of the capacitors, can be obtained. It is however necessary to know the power dissipated by the MOSFET and the heat sink and thermal pad resistors.

The average T_{case} can be them calculated as:

$$T_{case} = P_{dis} Real[Z_{6,8}] + T_{amb}. \tag{6}$$

An easy way to solve Eq. (6) is in the Laplace domain, where each term is easily calculated. The real impedance can be calculated as:

$$Real[Z_{6,8}] = R_{6,7} + R_{7,8}. \tag{7}$$

$P_{dis}(t)$ can be calculated as the product of multiplying the voltage in the MOSFET and the current that travels through it. The voltage with high impedance faults can be considered almost sinusoidal [3,30] and the Laplace transform is straightforward. The current waveform, however, is more complex to obtain as the arc current waveform changes when different arc models are used. However, it is a periodic waveform which maintains the polarity of the voltage. The absolute value of a sinusoidal waveform in this study is used together with a correction factor, K, which is calculated to achieve the same average power in the sinusoidal and the arc waveforms. For instance, K = 0.572 was used for Fault $N°$ 2 in Table 2.

Therefore, the current waveform can be approximated by using the following equation:

$$I_{arc}(t) \approx K \cdot A|sin(\omega t)|, \tag{8}$$

where A is the peak value of the current with the arc waveform.

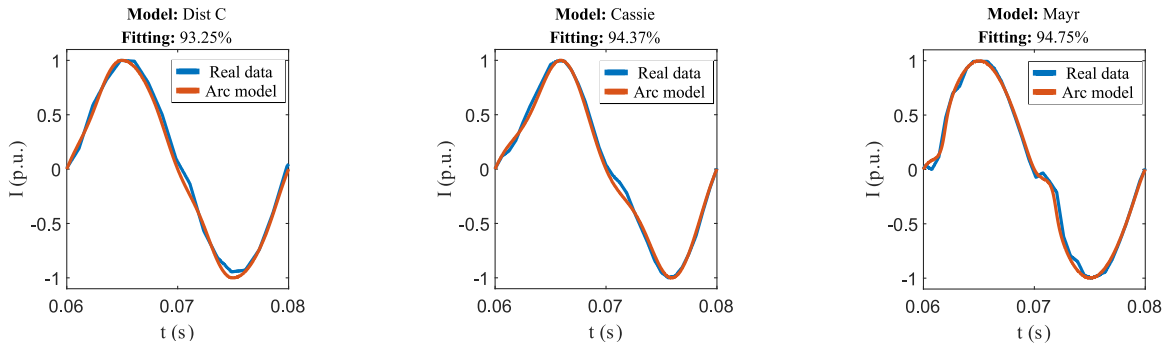
The voltage in the MOSFET is almost the absolute sinusoidal value, as the voltage drop in the shunt resistor (Fig. 2, R_{shunt}) is very small. The voltage can be expressed as:

$$V_{MOS}(t) = |V sin(\omega t) - R_{shunt} I_{arc}(t)|, \tag{9}$$

where V is the peak value of the voltage applied to the PCB.

Consequently, the power dissipated in the MOSFET can be expressed as:

$$P_{MOS}(t) = K \cdot A|sin(\omega t)|(|V sin(\omega t) - R_{shunt} K \cdot A sin(\omega t)|). \tag{10}$$



(a) Fault N^o 1. (b) Fault N^o 2. (c) Fault N^o 3.

Fig. 4. Arc current in p.u. values for different faults.

Table 2
Arc model parameters to emulate i-DEs network arcs.

Fault N^o	Dist C					Mayr				Cassie			
	DUR	EXT	OFS	IAE·10^{-3}	ISE·10^{-3}	τ	P_0	IAE·10^{-3}	ISE·10^{-3}	τ	U_c	IAE·10^{-3}	ISE·10^{-3}
1	0.0067	34.500	−48.02	**0.799**	**0.045**	0.00153	329.63	0.803	0.093	0.008087	37.32	0.912	0.202
2	0.0073	90.038	−42.24	0.744	0.051	0.00165	454.58	1.395	0.251	0.003127	38.62	**0.618**	**0.031**
3	0.0041	334.67	−29.97	0.641	0.067	0.00048	145.27	**0.597**	**0.041**	0.008760	37.40	1.345	0.188

Eq. (10) can be expressed in a compact form as:

$$P_{MOS}(t) = sin^2(\omega t)\underbrace{[K \cdot A \cdot V - R_{shunt}(K \cdot A)^2]}_{M}. \tag{11}$$

As all the terms inside the square brackets are constant, they can be simplified with the constant value M. The Laplace transform of (11) is:

$$\mathcal{L}\{P_{mos}(t)\} = M\frac{2\omega^2}{s(s^2+4\omega^2)}. \tag{12}$$

Substituting (7) and (12) into (6), MOSFET T_{case} can be obtained. By doing so, the equation that needs to be solved in the Laplace domain is:

$$T_{case}(s) = T_{amb}(s) + M\frac{2\omega^2}{s(s^2+4\omega^2)}\left(R_{6,7}+R_{7,8}\right). \tag{13}$$

Applying the inverse Laplace transform yields the time domain Eq. (14):

$$T_{case}(t) = T_{amb}(t) + M(R_{6,7}+R_{7,8})sin^2(\omega t). \tag{14}$$

The average temperature is determined by the average temperature of (14). It depends solely on the resistors of the thermal pad (Fig. 3, $R_{6,7}$) and the heat sink (Fig. 3, $R_{7,8}$). Thus, the worst case average temperature is a straightforward calculation, knowing the values of M and the resistors, $R_{6,7}$ and $R_{7,8}$.

Even after calibration, the Foster model maintains its inherent feature of a simplified representation of the real system, so it cannot fully capture all the complexities. However, calibration based on experimental data significantly improves the accuracy and the utility of the model for thermal analysis and design.

4. Simulation results

Some simulation tests were performed, in order to validate the proposed system.

4.1. Simulation of electric arc models

Matlab-Simulink was used to validate the system and to extract the arc model parameters with the optimization algorithm. To do so, Mayr, Cassie and Dist-C arc models were selected, but other models could be used in the proposed system. The genetic algorithm in [37] was used to obtain the parameters of each model that minimizes (5).

From the numerous single-phase faults that have been analyzed, three of them have been selected as an application example. The parameters obtained after minimizing (5) are presented in Table 2, where the model depicting the lowest value of (5) for each case stands out in bold. As can be seen in Table 2, no single arc model can be said to be the most suitable in each and every case.

The arc models with the optimal parameters that minimize (5) are performed and compared with the data provided by i-DE [34] in Fig. 4 where the fault current measurements together with the best arc model current are displayed. In all cases, the fitting % is calculated. They closely resemble real arc measurements, with a maximum fit percentage of 94.75% in the best case and 93.35% in the worst case.

Table 3
Foster model values of the board design.

Resistor	Value [mΩ]	Capacitor	Value [F]
R_1	3.100	C_1	0.0027
R_2	0.300	C_2	0.1439
R_3	11.30	C_3	0.0192
R_4	81.60	C_4	0.6709
R_5	138.1	C_5	1.7040
R_6	231.6	C_6	0.2500
R_7	300.0	C_7	2.0000

4.2. Thermal limits simulations

The power limits were verified through the implementation of the Foster model presented in Fig. 3 using LTspice software. The MOSFET values were obtained from the spice model of the manufacturer and the resistances of the heatsink (Fig. 3, $R_{6,7}$) and thermal pad (Fig. 3, $R_{7,8}$) were obtained from their data sheets. The values of thermal capacitance, $C_{6,7}$ and $C_{7,8}$, were calculated to achieve a total thermal time constant of one minute, which is a typical value for a heatsink with forced air flow [43]. All the values of the Foster model are presented in Table 3. It is important to highlight that the intermediate nodes of the Foster network lack physical meaning. However, the estimated average T_{case} temperature can be used, as the power oscillations are

Table 4
Case temperature in the LTspice simulation.

T_{case} [°C]	Voltage V_{peak}^{input} [V]												
Current I_{peak} [A]	25	50	75	100	125	150	175	200	225	250	275	300	325
0.5	24.78	26.76	28.72	30.70	32.68	34.65	36.61	38.60	40.55	42.50	44.45	46.45	48.45
0.75	25.65	28.60	31.55	34.50	37.45	40.46	43.38	46.35	49.30	52.30	55.25	58.25	61.20
1	26.50	30.43[a]	34.37	38.34	42.30	46.25[a]	50.18	54.10	58.08	62.00	66.00	69.95	73.90
1.25	27.33	32.25	37.20	42.15	47.10[a]	52.00	56.95	61.90	66.80	71.75	76.70	81.70	86.65
1.5	28.13	34.07	40.00	45.90	51.84	57.75	63.70	69.60	75.60	81.50	87.40	93.30	99.20
1.75	28.92	35.82	42.75	49.65	56.58	63.50	70.35	77.10	84.15	91.08	98.05	105.00	111.90
2	29.70	37.59[a]	45.50	53.40	61.30[a]	69.20[a]	77.10	85.00	92.80	100.80	108.70	116.60	124.50
2.25	30.45	39.32	48.20	57.05	65.90	74.80	83.70	92.60	101.40	110.30	119.20	128.10	136.85
2.5	31.20	41.04	50.95	60.75	70.60	80.50	90.30	100.20	110.00	119.85	129.70	139.50	149.35
2.75	31.87	42.72	53.58	64.40	75.20	86.05	96.90	107.80	118.50	129.45	140.25	151.25	161.60
3	32.59	44.42	56.25	68.00	79.90	91.60	103.45	115.40	127.25	139.00	150.75	162.60	174.40

[a] These values have been tested experimentally in Table 6.

Table 5
Case temperature obtained with Eq. (14).

T_{case} [°C]	Voltage V_{peak}^{input} [V]												
Current I_{peak} [A]	25	50	75	100	125	150	175	200	225	250	275	300	325
0.5	24.88	26.78	28.68	30.59	32.49	34.39	36.29	38.20	40.10	42.00	43.90	45.80	47.71
0.75	25.80	28.66	31.51	34.36	37.22	40.07	42.92	45.78	48.63	51.48	54.34	57.19	60.04
1	26.72	30.52[a]	34.33	38.13	41.93	45.74[a]	49.54	53.35	57.15	60.96	64.76	68.56	72.37
1.25	27.62	32.37	37.13	41.89	46.64[a]	51.40	56.15	60.91	65.66	70.42	75.17	79.93	84.68
1.5	28.51	34.22	39.92	45.63	51.34	57.04	62.75	68.46	74.16	79.87	85.57	91.28	96.99
1.75	29.39	36.05	42.71	49.36	56.02	62.68	69.34	75.99	82.65	89.31	95.97	102.62	109.28
2	30.26	37.87[a]	45.48	53.09	60.69[a]	68.30[a]	75.91	83.52	91.13	98.74	106.35	113.95	121.56
2.25	31.12	39.68	48.24	56.80	65.36	73.92	82.48	91.04	99.60	108.15	116.71	125.27	133.83
2.5	31.97	41.48	50.99	60.50	70.01	79.52	89.03	98.54	108.05	117.56	127.07	136.58	146.09
2.75	32.80	43.26	53.73	64.19	74.65	85.11	95.57	106.03	116.50	126.96	137.42	147.88	158.34
3	33.63	45.04	56.45	67.87	79.28	90.69	102.11	113.52	124.93	136.34	147.76	159.17	170.58

[a] These values have been tested experimentally in Table 6.

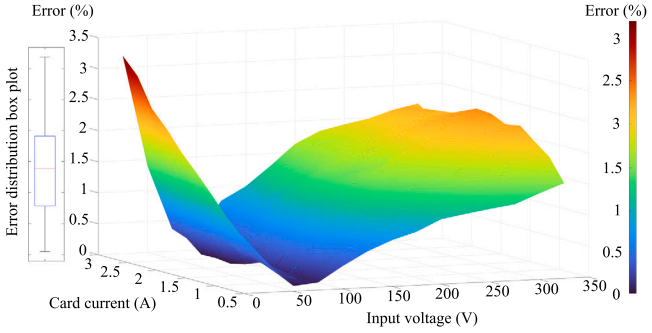


Fig. 5. Error % between Tables 4 and 5.

of higher frequency compared with the slower thermal dynamic of the heat sink. T_{case}, obtained with the Foster model, is then compared with the value of (14). The T_{case} values obtained in the simulations for different voltage and current levels are presented in Table 4, using the arc waveform of Fault $N°2$ Table 2. The temperatures obtained with Eq. (14) for the same fault are shown in Table 5. Both tables depict similar values. The differences are shown in Fig. 5, for clearer appreciation of the differences between Table 4 and Table 5. The maximum error was 3.19% and the median error was 1.44%. It can therefore be concluded that the simplification in Eq. (8) is correct.

5. Experimental results

Some experimental tests were conducted, the results of which demonstrated the reliable performance of the proposed system in an LV laboratory Figs. 6(a) and 6(b). The platform included: (a) Cinergia GE&EL-15 voltage source; (b) electronic board designs (electrical diagram in Fig. 2); (c) series resistors to dissipate power, if needed; (d) OpalRT 4510 where the arc model is created, and (e) YOKOGAWA DL850EV ScopeCorder, to monitor the board currents and voltages.

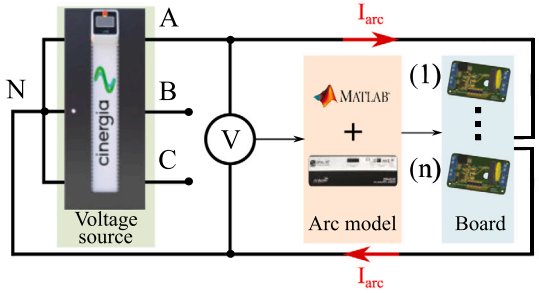
5.1. Validation of the electric arc models and PCB

Arc models obtained in Section 4 were uploaded onto the OpalRT 4510 Rapid Control Prototyping platform Figs. 6(a) and 6(b), to test the generation of electric arcs in the PCB. Once calculated, the numerical value of the reference current was digitalized in a PWM 100 kHz signal inside the FPGA unit. In this way, a pulse width modulated signal was generated and transmitted through fiber optics, isolating the OpalRT 4510 from the PCB arc generator. The resulting pulse train was the input value for an auxiliary board that converted the optical pulse train into an electrical one. The electrical pulse train contains the shape of the arc current in its modulation that will be the reference input for the arc emulator. Subsequently, a low-pass filter was employed to reproduce the arc reference (Fig. 2, ①I_{ref}). The main components of the implemented PCB are: (a) MOSFET: IXTH40N50L2; (b) Operational amplifier: LT1490 A; (c) Push pull DC/DC QS5Y1TR; (d) Diode bridge: KBU1510; (e) Varistor: WE-VD 20 mm 860 pF.

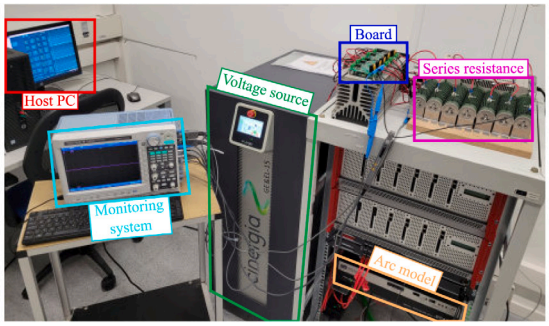
The PCB is supplied with varying voltage values from the Cinergia power source Figs. 6(a) and 6(b) and it emulates a single-phase arc between one of the phases and the neutral [26].

Although the PCB design specifies a maximum of I_{peak} = 2 A with an input voltage of V_{peak} = 125 V, if higher currents are required, more PCBs can be used in parallel to the previous ones. The PCB array in parallel was tested on the test bench, depicted in Fig. 6(b), where an array of five PCBs, depicted in Section 3.2, were mounted on a heat sink, to verify their operation.

The same tests that were simulated in Section 4.1 were carried out with five PCBs in parallel configuration. Although the original design of the PCB array was sufficient (I_{peak} = 2 A and input voltage V_{peak} = 125 V), a safety margin must be applied to ensure that the temperatures are still within acceptable values. The input voltage for the test was



(a) Experimental platform scheme.



(b) Experimental platform in the LV facility.

Fig. 6. Experimental platform scheme and real platform in the LV.

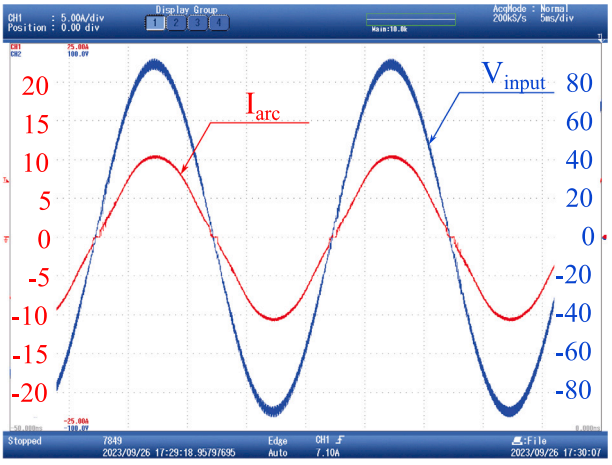


Fig. 7. Arc current and voltages in fault $N°$ 1 Dist-C model.

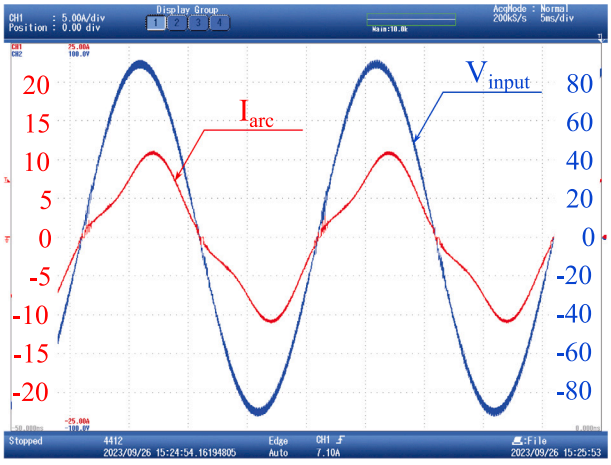


Fig. 8. Arc current and voltages in fault $N°$ 2 Cassie model.

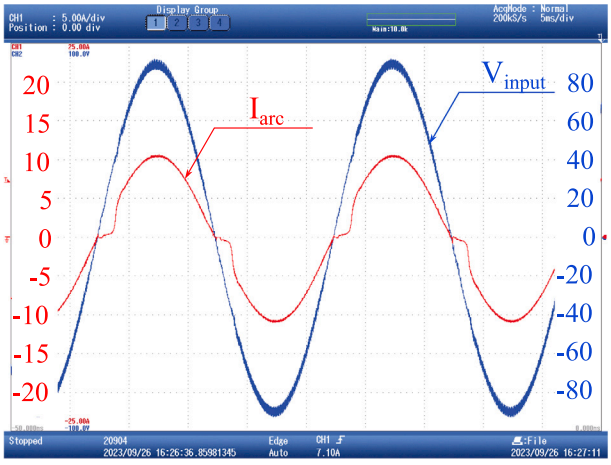


Fig. 9. Arc current and voltages in fault $N°$ 3 Mayr model.

therefore selected at V_{peak} = 90 V as the previous safe operational scenario was only valid for a single PCB. The current level was not modified, so the current of each one was maintained at I_{peak} = 2 A, yielding a total current level of I_{peak} = 10 A. Both the waveform of the total current and the input voltage are presented in Figs. 7–9. Note the requirement for the input voltage and arc current to have the same polarity. The current on the circuit boards was slightly higher than the specified value of 10 A, because the shunt resistor was not exactly 1 Ω. In the experimental setup, the shunt resistor was formed of 5 resistors, each of 4.7 Ω Fig. 2, yielding a total R_{shunt} = 0.94 Ω. The current must therefore be higher than the set point, I_{ref}/R_{shunt} times, in order to obtain the set voltage drop. However, the resulting current maintained the arc shape in the simulation models Fig. 4.

As the arc is modeled as a variable resistor combined with a fixed resistor, there must be a minimum voltage across the MOSFET to carry the desired current. Therefore, the voltage drops in the diode bridge, the shunt resistor, and the series resistor (if needed) must be taken into account. Neglecting the resistor of the wires and PCB tracks, the minimum voltage can be calculated as:

$$V_{min} > 2(V_F^{diode} + R_{on}^{diode} I_{R_{shunt}}) + I_{R_{shunt}}(R_{shunt} + R_{DS(on)}^{MOSFET} + R_{series}) + \alpha, \quad (15)$$

where α is an extra term added as a safety margin. The reference current was adjusted, to avoid current spikes when the voltage crossed zero. If (15) was not fulfilled, the current reference was set to 0. This phenomenon can be observed in Figs. 7–9, where at the zero crossing of the voltage, the condition (15) is not fulfilled, and the current is brought to zero. A safety margin of $\alpha = 2$ V was used in the experimental tests, to ensure that the minimum voltage was reached.

5.2. Validation of the Foster thermal model

The implemented thermal Foster model was also experimentally tested. In doing so, T_{case} was measured for several experimental tests using a single PCB with a 300 mm long heat sink and a K type thermocouple. Different current and voltage values were tested, in order to validate the model over a wide range of values. The test results Table 6 were compared with the average values of Eq. (14) and simulations of the Foster model developed in LTspice with the

Table 6
Case temperature values under the test conditions.

Case	$I_{peak}[A]$ $V_{peak}^{input}[V]$	T_{case}					T_{junct}
		Experimental T [°C]	LTspice model T [°C]	Average value of (14) [°C]	Error with LTspice [°C]	Error with (14) [°C]	LTspice model T [°C]
1	$I_{peak}=2$ $V_{peak}^{input}=90$	51.50	50.30	50.04	1.20	1.46	64.55
2	$I_{peak}=2$ $V_{peak}^{input}=125$	60.50	61.30	60.69	−0.80	−0.19	81.50
3	$I_{peak}=1{,}25$ $V_{peak}^{input}=90$	41.30	40.15	39.98	1.15	1.32	49.20
4	$I_{peak}=1{,}25$ $V_{peak}^{input}=125$	47.50	47.10	46.64	0.40	0.86	59.70
5	$I_{peak}=1$ $V_{peak}^{input}=150$	48.60	46.25	45.74	2.35	2.86	58.60
6	$I_{peak}=1$ $V_{peak}^{input}=50$	32.00	30.43	30.52	1.57	1.48	34.40
7	$I_{peak}=2$ $V_{peak}^{input}=50$	38.00	37.59	37.87	0.41	0.13	45.35
8	$I_{peak}=2$ $V_{peak}^{input}=150$	69.80	69.20	68.30	0.60	1.50	93.60

arc model of Fault $N°$ 2 Table 2. The error between the measured and the simulated temperatures was sufficiently low with a maximum difference of 2.86 °C Table 6. It was therefore concluded that the Foster network was valid for calculating the T_{case} average values.

Moreover, if the same calculations are made for higher input voltages, series resistors to dissipate overheating of the resistors can be added to the PCB. In that sense, for the case: $V_{peak}^{input}=325$ V, $I_{peak}=2$ A if no series resistor is added, the MOSFET T_{case} will be $T_{case}=121.56$ °C according to Table 5. Using the same procedure, the modeled T_{junct} value will be 170.49 °C. Those temperatures exceeded the maximum limits for the MOSFET. It was therefore necessary to add resistors in series with the PCB. As an example, a series resistor of $R=110\ \Omega$ was used. The estimated T_{case} was 73.33 °C, while the T_{junct} was 95.58 °C. The same test was experimentally conducted, yielding a case temperature of $T_{case}=69.50$ °C. Considering the above, the temperature decrease was noteworthy. It brings the PCBs down to acceptable temperature levels compared to when series resistors are not present.

Therefore, the cards can be used within higher power ranges, although the trade-off is loss of manageability, as series resistors with the circuit become necessary to dissipate the excess heat that may be generated. Nevertheless, the current remains non-linear while maintaining the desired amplitude, depending on the arc model used. The formula in Eq. (14) is used to estimate the temperature in a straightforward way and the series resistor value can be adjusted, so that the temperature of the MOSFET is always maintained within safe operational parameters.

6. Discussions

In the following section, the most frequently used methods for LV fault emulations are presented and compared with the solution proposed in this article. Those methods are divided into: direct resistors, arc generator devices [44], and arcs generated due to insulation faults [28].

The proposed system can reproduce the non-linearities inherent in the arc current. A notable feature is the system's capacity to employ either a variety of arc models or to reproduce previous experimental data bridging the gap between theoretical modeling and real-world applications. This capability to reproduce the current waveform is a feature that cannot be achieved with the previously proposed systems.

The use of resistors to reproduce an electrical fault is a simple and common technique used in literature. However, the currents that are generated when considering resistors are completely proportional to the applied voltage, and can never reproduce non-linearities present in real arc phenomena. The use of two electrodes with an airgap between them is another common way of emulating electrical arcs in LV prototypes and facilities. The main disadvantage of that method is the random nature of the arcs that are provoked and the fire risk generated due to sparks. This risk is also present when two cables with a gap in the isolator are considered, in order to emulate an insulation fault that causes real electrical arcs.

Table 7
Table of comparison with other LV fault emulation.

	Resistor	Arc generator	Insulation break arc	Proposed system
Programmable current waveform	NO	NO	NO	YES
Non linearity	NO	YES	YES	YES
Fire hazard elimination	YES	NO	NO	YES
Experimental data reproduction	NO	NO	NO	YES

The commitment to safety built into the proposed system is one of its key advantages, as it eliminates fire hazards avoiding the spark generation. Another outstanding advantage is its versatility, as it can reproduce theoretical arc models, and arcs based on real measurements taken from the distribution grid. Furthermore, the proposed design is modular and offers the opportunity to increase the current levels of the emulated electrical arc by means of parallelization, as has been experimentally tested. Finally, the main limitation of the proposed design is that it cannot be used to generate current values other than zero when the input voltage is zero, which prohibits any emulation of inductive currents.

A summary explanation of the main advantages and disadvantages is given in Table 7.

7. Conclusions

In this paper, a PCB capable of emulating both the arc shapes of various arc models and experimental data from the grid has been presented. The proposed model can be used on LV test benches to safely replicate a wide variety of electric arc currents, ensuring the safety of both staff and equipment. System functionality and reliability have been validated through a combination of both simulations and

experimental results. Its cost effectiveness ensures the affordability of the application for researchers interested in its use.

The proposed solution has a modular design, which makes it adaptable to a wide range of currents. Current levels up to 10 A have been successfully created in different LV levels. Furthermore, a detailed flow chart has been provided for calculating the number of PCBs required for a given current level and input voltage. The lack of a secure device to reproduce the current non-linearities in a safe way motivated the authors to develop the proposed system.

As future work, the proposal will be extended to higher current and voltage levels, so that the system may be used in applications with higher power requirements. Another future line or research might be to implement a new hardware design to obtain a characteristic arc voltage fault.

CRediT authorship contribution statement

Asier Davila: Conceptualization, Methodology, Data curation, Investigation, Software, Validation, Writing – original draft, Writing – review & editing. **Alberto Otero:** Investigation, Validation, Conceptualization, Writing – review & editing. **Estefania Planas:** Supervision, Conceptualization, Project administration, Writing – original draft, Writing – review & editing. **Jose Antonio Cortajarena:** Supervision, Conceptualization, Writing – review & editing. **Antoni Arias:** Supervision, Conceptualization, Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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